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(54) IMPROVEMENTS IN AND RELATING TO METHODS OF AND APPARATUS FOR CHARGING ACCUMULATORS

(71) We, THEO BIENNING ELEKTROTECHNIK UND ELEKTRONIK GMBH & CO. KG. a German Kommandit Gesellschaft of Munsterstrasse 135-137, 4290 Bocholt, Federal Republic of Germany, do hereby declare the invention, for which we pary that a patent may be granted us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

The invention relates to methods of and apparatus for charging electrical accumulators.

According to the invention there is provided a method of controlling the charging of an accululator, comprising the steps of measuring the charging current at regular intervals, comparing the values of successive measurements to determine the difference in the values comparing the determined difference with a reference difference and halting the charging operation when the determined difference fails to exceed the reference difference on at least two occasions.

According to the invention there is further provided apparatus for controlling the charging of an accumulator, comprising means for sensing the charging current drawn by an accumulator being charged and generating an output pulse train having a pulse repetition rate related to the magnitude of the current, a reversible counter, means for feeding the pulse train at regualr intervals, for the same predetermined duration each time, to the counter so that the number of pulses received by the counter corresponds to the charging current, means for causing the counter to count in one direction at the end of each alternate interval and count in the opposite direction at the end of each intervening interval so that the count registered by the count at the end of each intervening interval represents the change in charging current from one interval to the next, and means for sensing when the count registered by the counter after counting in the said opposite direction is less than a predetermined datum count on at least two occasions to produce a signal to halt the charging of the accumulator.

A method of and apparatus for charging electrical accumulators and according to the invention will now be described, by way of example, with reference to the accompanying drawings in which:

Figure 1 is a block diagram of the apparatus; and

Figure 2 is a circuit diagram of the apparatus of Figure 1.

The apparatus shown in Figure 1 is arranged to control the charging of an electric accumulator (not shown). A d.c. charging source (not shown) is arranged to feed the accumulator through a switching arrangement 100 and through a series resistor 102. The voltage appearing across the resistor 102 represents the charging current drawn by the accumulator. The resistor 102 is advantageously selected to provide a variation in potential from 0 to 60 mV in response to a variation of charging current between zero and a maximum value for the accumulator to be charged.

The voltage appearing across the resistor 102 is sensed by a voltage to frequency converter 104 whence it is fed simultaneously to the inputs of a display unit 106 and a reversible counter 108. The unit 106 and counter 108 are gated at intervals of 20 minutes by pulses from a clock pulse generator 110 and when gated the output from the converter 104 is displayed by the unit 106 and stored by the counter 108. The counter is arranged to count up on every alternate storage cycle and count down on every intervening cycle, the counter being cleared after every intervening cycle.

A comparator 112 is gated by the clock pulse generator to make a comparison between a reference count and the value of the count in the counter at the end of each intervening cycle. This represents the difference between successive counts.

If the comparator 112 does not sense a difference in charge currents in excess of 0.3%,

a pulse is generated and fed to a delay unit 114. If the delay unit 114 receives another such pulse after the next clock pulse from the clock pulse generator 110, a pulse is generated to trigger a stop unit 116. When triggered the stop unit 116 actuates a stop-start store 118 which in turn operates the switching arrangement 100 to disconnect the accumulator from the charging source. At the same time the clock pulse generator 110 is disabled.

An excess current sensor 120 monitors the value of the charging current stored by the counter 108, and when the value exceeds that of the maximum charging current, a pulse is generated to trigger the stop unit 116 which again will act in the described manner.

The apparatus is powered from a set of d.c. supply terminals 122 connectable to the battery being charged. An ON/OFF unit 124 including a normally closed reset key is operable to energise the individual units of the apparatus as well as to supply an enabling pulse to the pulse generator 110 and the stop-start store 118. Upon receipt of the enabling pulse the pulse generator 110 begins to generate pulses and the stop-start store 118 operates the switching arragement 100 to supply charging current to the battery. A fourteen hour safety switch 126 is connected to the terminals 122 and after a fourteen hour period of continuous energisation generates a trigger pulse to actuate the stop-start store 118 to cause the switching arrangement 100 to disconnect the accumulator from the charging supply.

Thus in operation after the start of the charging operation, the charging current is detected by the analogue-digital converter, and the digital values of two consecutive measurements results are then compared. The first measurement occurs twenty minutes after the start of the charging operation. The measuring period itself amounts to 1000 milli-seconds. The converter frequency is so selected that 1000 cycles per second are counted at maximum charging current flow. These measurements are repeated every twenty minutes throughout the whole charging operation. The comparator acts to compare the consecutive measurements and derive a percentage difference between the two and a pulse is generated when the preset minimum difference of 0.3% is not achieved. The occurrence of two such pulses following consecutive comparisons indicates that the charging current is practically constant, so that the charging operation is terminated.

The charging operation is also terminated when the charging current becomes excessive because of a defective accumulator or in the case of the wrong accumulator being connected to the charging plant, for example where the accummulator has less than the required number of cells. To check the charging current, an indicator system displays the charging current digitally. A display of this kind preferably occurs in one-second cadence.

After disconnecting the accumulator from the charging plant, the last charging current to flow remains on display, so that a subsequent check is possible. If a power failure occurs during the charging operation, the switch 124 is switched on again automatically after restoration of the power. In the same way, the charging operation may be temporarily interrupted by means of the key (not shown). The state of the charging operation is advantageously indicated by pilot bulbs (not shown). For example the illumination of a green pilot bulb would indicate the termination of charging, the illumination of a red pilot bulb would indicate charging in progress and the illumination of both yellow and green bulbs would indicate a shut-down due to excess charging currents. As soon as the accumulator is separated from the charging plant after completion of the charging operation, the charging current display is extinguished. The charging operation is switched ON automatically 5 seconds after an accumulator is connected to the terminals of the charging plant.

The fourteen hour timing circuit acts as a safety cut-off in case the charging control circuit were to fail for any reason. The timing circuit causes a disconnection of the accummulator from the charging plant after 14 hours, and the supply of current to this timing circuit is provided from the accumulator voltage, so that its condition is not altered in case of a power failure. However, the timing circuit does not continue to run during the period of a power failure, but starts up again only after restoration of the power supply voltage. In the event that the timing circuit triggers the termination of the charging operation, the illumination of a yellow bulb on its own indicates this action has occured.

Figure 2 shows the block diagram of Figure 1 in more detail.

The voltage appearing across the resistor 102 (see Figure 1) is applied to the input of an integrating amplifier 1 wherein it is amplified to an extent sufficient to drive a voltage-to-frequency converter 2. The zero setting of the integrating amplifier 1 is performed by adjusting a potentiometer 70. The amplification factor of the integrating amplifier 1 is set at "50". With maximum output voltage, from the integrating amplifier, the maximum voltage required to be fed to the voltage-to-frequency converter 2 is adjusted by means of a potentimeter 71. The voltage-to-frequency converter 2 acts to produce a signal having a frequency related to the output voltage of the integrating amplifier (and therefore to the charging current) and feeds this signal to three counters 17, 18, 19 connected in cascade via a gate 41.

The accumulator to be charged feeds a constant current circuit comprising a transistor 74, resistors 75 and 77, and a Zenor diode 76. The output voltage of the constant current

circuit is stabilized by a Zenor diode 83. The voltage across the Zenor diode 83 is fed to a Schmitt-Trigger 28 via a delay circuit. The delay circuit includes a capacitor 84 and resistor 85 and acts to delay the application of a voltage to the Schmitt-Trigger 28 by approximately 5 seconds after the accummulator is connected to the constant current circuit. The capacitor 84 ensures that in the event of brief interruption of the current supply from the accumulator, the Schmitt-Trigger 28 remains triggered. The capacitor 84 is discharged via a diode 86. After the 5 second delay from switch ON has elapsed, a high potential appears at the output terminal of the Schmitt-Trigger 28. This trips a flip-flop 27 (which at switch ON provided a low potential at its output) into its other state in which it provides a high potential at its output. The high potential outputs of the Schmitt-Trigger and the flip-flop condition a NAND gate 63 to fall from a high output to a low output and so switch a transistor 64 ON. The high output from the Schmitt-Trigger switches OFF a transistor 87 which drives an opto-coupler 12. The transistor 64 when switched ON drives another opto-coupler 26 which in turn transmits a signal to a transistor 65 to switch the transistor 65 ON. The opto-coupler 12 when driven trips a Schmitt-Trigger 47 to generate a high output and thus through Schmitt-Trigger 46 produces a reset signal to inhibit any counting operation from taking place. Thus at the end of the inital 5 second delay, when the opto-coupler ceases to be driven the reset signal is removed and counting by the various counting circuits can start as will be hereinafter described.

When a low potential appears at the output terminal of one Schimitt-Trigger 46, a high potential appears at the output of an OR gate 33, and six cascade-connected counters 5 to 10 of the clock pulse generator 110 are enabled. Via a secondary winding of a transformer 72 and a terminal 100, a signal Vcc of mains frequency derived from the mains acts to trigger a Schmitt-Trigger 68 to feed clock pulses to the cascade-connected counters 5 to 10. A period of 20 minutes elapses before the outputs of counter 7 and counter 10 simultaneously generate an output. When this occurs a gate 34 is enable and a pulse is passed via NAND gate 42 to a flip-flop 14. The duration of this pulse is 1 second. Upon being triggered the flip-flop 14 enables three cascade-connected decade counters 17 to 19 which consitute the reversible counter 108. Pulses from the voltage to frequency converter 2 are fed via NAND gate 41 into the counter 17. The NAND gate 41 is enabled since the low potential at the output of an AND gate 49 is fed via an inverter 44 to the NAND gate 41 as a high potential.

The three counters 17 to 19 which can count up to a maximum of 999 pulses count the incoming pulses for the period of 1 second, at the end of which period the flip-flop 14 reverts to its original state. After another 20 minutes, when the output of the gate 42 changes to high potential again, the counters 17 to 19 are released to count again but this time in reverse, i.e. to count down. The count again lasts for a period of 1 second and the extent of the downward count will represent the latest charging current drawn by the accumulator. If this current is less than that just previously measured, the residual count in the counters will be indicative of the extent of this.

The counters 18 and 19 are so programmed via NOR gates 51, 52 that a high potential appears at the output terminals of the NOR gates 51, 52 only when the reading from these two counters 18, 19 is zero. Thus, if 999 pulses are counted during the first measuring cycle, these two counters 18, 19 are at zero only when at least 990 pulses have been counted off in reverse order. When the counter reading reaches the value of 996 pulses during counting down of the count in the counter an AND gate 50 connected directly to two stages of the counter and indirectly via an inverter 45 to a third stage will register this and generate a high potential. Under these conditions the outputs of the two NOR gates 51 and 52 will also register a high potential as will also the output of the flip-flop 14 and thus the AND gate 49 is enabled.

The high output generated by the NAND gate 44 blocks the gate 41 from passing any more pulses to the counter. At the end of the 1 second counting period, the flip-flop 14 changes state so that the AND gate 49 is disabled and reverts to generating a low potential. The pulse thus generated by the AND gate 49 is sensed and stored in a counter 20. At the end of the measuring cycle, when the flip-flop 14 reverts to its original state a monostable device 15 is triggered to pass a reset signal through an OR gate 39 and an inverter 40 to reset the three counters 17 to 19.

Thus as long as the measurement value of each cycle is smaller than the value of the preceding cycle by at least three pulses counting cannot proceed in the counter 20 since the output of the gate 49 does not change. If, however, the difference between the values of two successive measuring cycles is three pulses or less, the output of the gate 49 changes and is registered by the counter 20. This action usualy occurs towards the end of the charging period for the accumulator when the difference between the values of two successive cycles tends towards zero. A NAND gate 55 has one input connected to the output of the counter 20 through an OR gate 53 so that when the counter reaches a count of two the output of the counter 20 will rise from a low to a high level and a signal will be passed by the NAND gate 55 to switch OFF a transistor

66 which in turn de-energises a relay 69 controlling the charging operation of the accumulator (not shown). A luminescent diode 81 connected in parallel with the emitter-base of the transistor 81 which when illuminated indicates a "charging in progress" condition, is switched OFF when the transistor 66 is switched OFF.

The output of the OR gate 53 also feeds one input of a NAND gate 54 while at low potential, the output of the NAND gate 54 enables the NAND gate 42 to pass clock pulses.

When the count of the counter 20 reaches a count of 2, its output as stated previously rises to a high potential and a signal is fed via OR gate 53 and NAND gate 54 to disable the NAND gate 42. The measuring programme is thereby switched OFF. A luminescent diode 82 connected to the output of NAND gate 54 lights up and indicates "charging completed".

When termination of the charging operation is indicated by the luminescent diode 82 a key 78 can be operated to recommence the charging operation. When the key 78 is closed, the input of a Schmitt-Trigger 48 is grounded and the Schmitt-Trigger acts to set flip-flop 13 to zero. The Schmitt-Trigger 46 is thereupon disabled and a reset signal is generated to reset the counters 5 to 10, the counter 20 and the counters 17 to 19 to zero. The reset signal is fed to OR gate 55 which is disabled and immediately generates a low output potential to switch the transistor 66 ON again and thereby re-energise the relay 69. The luminescent diode 81 indicating "charging in progress" is simultaneously re-lit. Renewed actuation of the key 78 causes the flip-flop 13 to revert to its original state and the reset signal is discontinued so that the charging operation is allowed to resume.

If the count of counters 17, 18, 19 exceeds a count of 999 a storing flip-flop 21 is caused to change state. The output of the storing flip-flop 21 is fed through the OR gate 53 and AND gate 55 to switch OFF the transistor 66 and thereby de-energise the relay 69. At the same time, the luminescent diode 81 indicating "charging in progress" is extinguished, and the luminescent diode 82 indicating "charging completed" and a luminescent diode 79 indicating "excessive current" both light up. Since the excessive current indicated probably represents a defect, the storing flip-flop 21 should be reset only when the accumulator is disconnected from the charging plant.

The safety cut-off (14-hour delay circuit) comprises a Schmitt-Trigger 22, counters 23, 24, 25 and gates 56, 57, 58, 59, 60, 61. A signal having a mains frequency component and derived from the secondary winding of the transformer 72 is fed via terminal 200 to the Schmitt-Trigger 22. The Schmitt-Trigger thus generates rectangular pulses which are fed to the counters 23 to 25 connected in cascade. When a number of pulses corresponding to the period of one second have been counted, a NAND gate 56 senses this and feeds a reset pulse via a NAND gate 57 to reset the counter 23 and increase the count of counter 24 by one. When the number of reset pulses corresponding to the period of 20 minutes have been counted by the counter 24, a NAND gate 58 senses this and feeds a reset pulse via NAND gate 59 to reset the counter 24 and increase the count of the counter 25 by one. When the number of reset pulses counted by the counter 25 correspond to the period of 14 hours, the NAND gate 63 senses this and feeds a signal via NAND gate 61 to the flip-flop 27. When the flip-flop 27 changes state in response to an output signal from the NAND gate 61, it feeds a signal through NAND gate 63 and inverter 62 to disable the NAND gates 57, 59 and 61 to halt any further counting by the counters 23, 24 and 25. At the same time, a transistor 64 is switched OFF and this in turn de-energises the opto-coupler 26. For its part, the opto-coupler 26 turns OFF the transistor 65 controlling the energisation of the relay 69, the relay thereupon discontinues the charging operation. A luminescent diode 80 is connected in series with the emitter-collector path of a transistor 67 and the transistor 67 is switched ON when the transistor 65 is switched OFF. As a result the diode 80 lights up to indicate a safety cut-out action.

The supply of current for the system described is provided exclusively from the accumulator voltage and is independent of the supply by mains voltage. If the mains voltage fails however, the counting operation is interupted during the period of failure, because the mains frequency is used to drive the Schmitt-Trigger 22. The delay circuit continues to count after restoration of the mains voltage.

A display unit having a four figure display 29 to 32 is connected to receive the same pulses as are received by the counters 17, 18, 19. The pulses are fed to the display through an AND gate 38 which is enabled during a measurement period of 1 second by an output pulse from the counters 5 to 10 fed to the AND gate 38 via an AND gate 35. The display includes a counter, a decoder, a driver and 7-digit indicator element for each figure to be displayed. The input terminal of the gate 37 is connected via inverter 97 to the output terminal of the Schmitt-Trigger 46 providing the reset signal. Therefore, the gate 37 is only enabled when the accumulator is connected in circuit. To cancel the displays 29, 30, 31, 32 during the counting operation, a transistor 88 is switched ON in response to an output from the gate 37. The output from the counter 7 which generates a pulse every second is connected to an input of the AND gate 35. The output of the AND gate 35 feeds an input of a monostable circuit 16 which acts to reset the counters of the display at the end of the counting.

It will be appreciated that the delay between measurement cycles can be varied by changing the tapping points on the counters 5 to 10, for example with the aid of a switch (not shown). The critical difference between successive measurements can be varied by appropriately varying the connection to the stages of the counter, again for example by means of a switch.

WHAT WE CLAIM IS:—

1. A method of controlling the charging of an accumulator, comprising the steps of measuring the charging current at regular intervals, comparing the values of successive measurements to determine the difference in the values, comparing the determined difference with a reference difference and halting the charging operation when the determined difference fails to exceed the reference difference on at least two occasions.

2. A method according to claim 1, wherein the measuring step comprises the step of converting the charging current into pulses having a repetition rate which varies as a function of the amplitude of the charging current and counting the number of pulses occuring during a period of predetermined duration.

3. A method according to claim 1 or to claim 2, including the step of delaying the first measurement step for a predetermined period after charging is initiated.

4. A method according to any one of claims 1 to 3, including the step of varying the length of time between said regular intervals and for varying said reference difference.

5. A method according to any one of claims 1 to 4, including the step of monitoring the determined difference and halting the charging operation when the difference changes polarity.

6. Apparatus for controlling the charging of an accumulator, comprising means for sensing the charging current drawn by an accumulator being charged and generating an output pulse train having a pulse repetition rate related to the magnitude of the current, a reversible counter, means for feeding the pulse train at regular intervals for the same predetermined duration each time to the counter so that the number of pulses received by the counter corresponds to the charging current, means for causing the counter to count in one direction at the end of each alternate interval and count in the opposite direction at the end of each intervening interval so that the count registered by the counter at the end of each intervening interval represents the change in charging current from one interval to the next, and means for sensing when the count registered by the counter after counting in the said opposite direction is less than a predetermined datum count on at least two occasions to produce a signal to halt the charging of the accumulator.

7. Apparatus according to claim 6, including means for monitoring the count by the counter and operative when the count recorded exceeds a predetermined maximum count, in response to an excess charging current being drawn, to produce a signal to halt the charging of the accumulator.

8. Apparatus according to claim 6 or to claim 7, including a display incorporating a display counter for receiving the said pulse train at the same regular intervals and for the same duration as the reversible counter to display a count of the pulses received and thus indicate visually the magnitude of the charging current.

9. Apparatus according to any one of claims 6 to 8, including a timer arranged to be energised by the accumulator and driven by pulses derived from an a.c. mains from which charging current for the accumulator is to be derived, the timer being operative in response to the expiry of a predetermined period of its operation by the a.c. mains to generate a signal for halting the charging of the accumulator.

10. Apparatus according to any preceding claim, including delay means for delaying the operation of the feeding means until a fixed period after the start of charging of the accumulator.

11. Apparatus for controlling the charging of an accumulator substantially as hereinbefore described with reference to Figure 1 of the accompanying drawings.

12. Apparatus for controlling the charging of an accumulator substantially as hereinbefore described with reference to Figure 2 of the accompanying drawings.

13. A method of controlling the charging of an accumulator substantially as hereinbefore described.

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Sheet 1

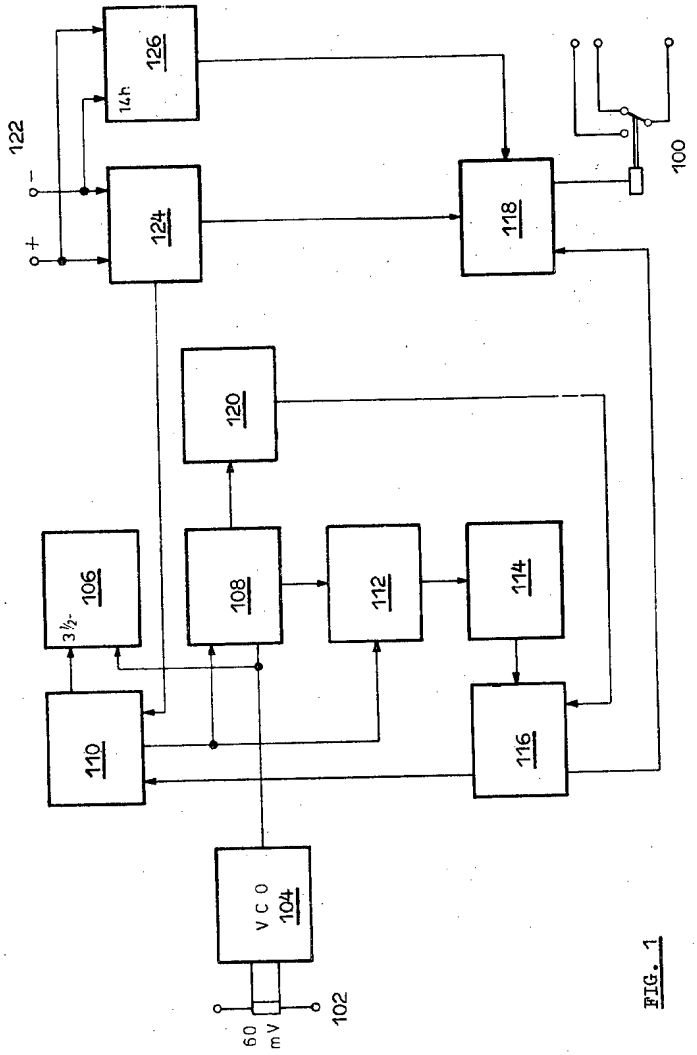

FIG. 1

1575543 COMPLETE SPECIFICATION

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Sheet 2

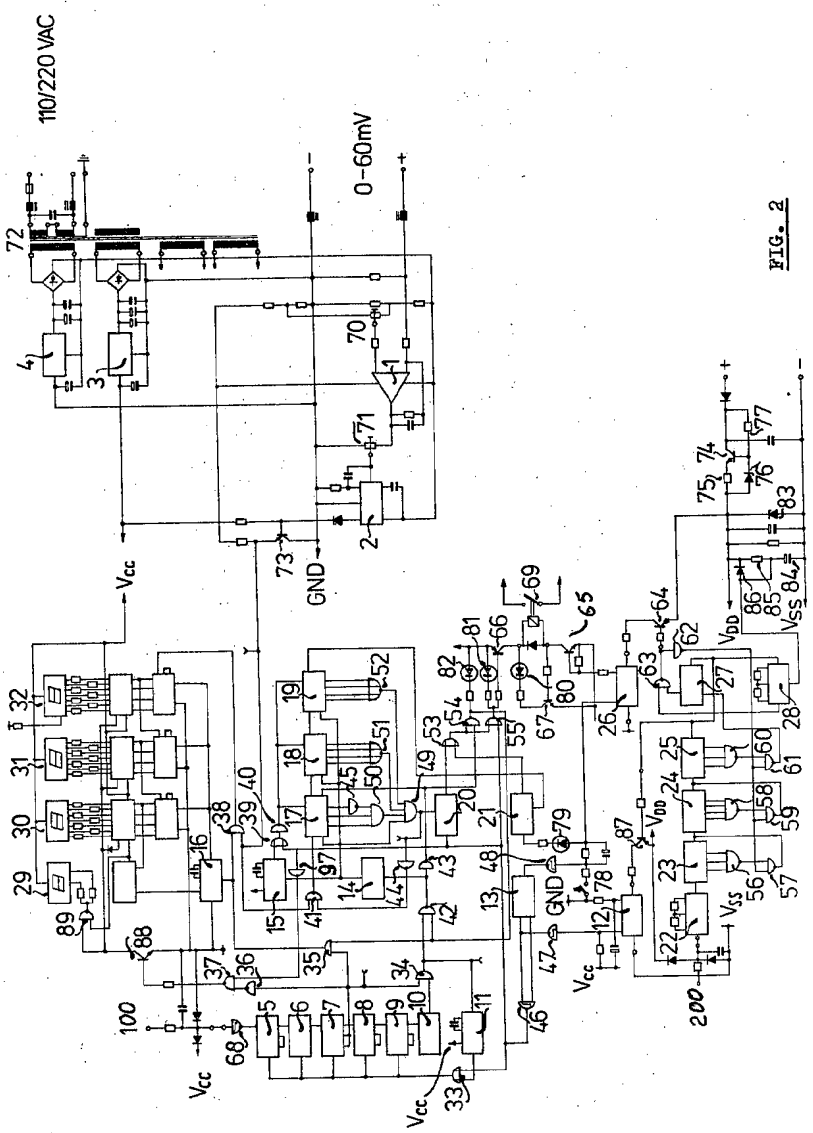

FIG. 2